

MS-7678

CPU:

uATX

Ver: 1.0

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4105

HD Audio Codec:RTL892

LAN:RTL 8111E 10/100/1000

SIO:FIN71889ED

Flash ROM: 32 Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 ISL6364CRZ 4+1-Phase

CPU+GPU

Controller:uP6138

CPU VTT CPU SA

Controller:uP6138

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

SATA3.0X1 + e-SATA X1(MARVELL9128_COLAY_E9172)

USB2.0 RearX4 Front x8(PCH&BC Charge & i Charge)

USB3.0 RearX2 (NEC USB3.0)

1394 Controller - VT6315N-CE

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

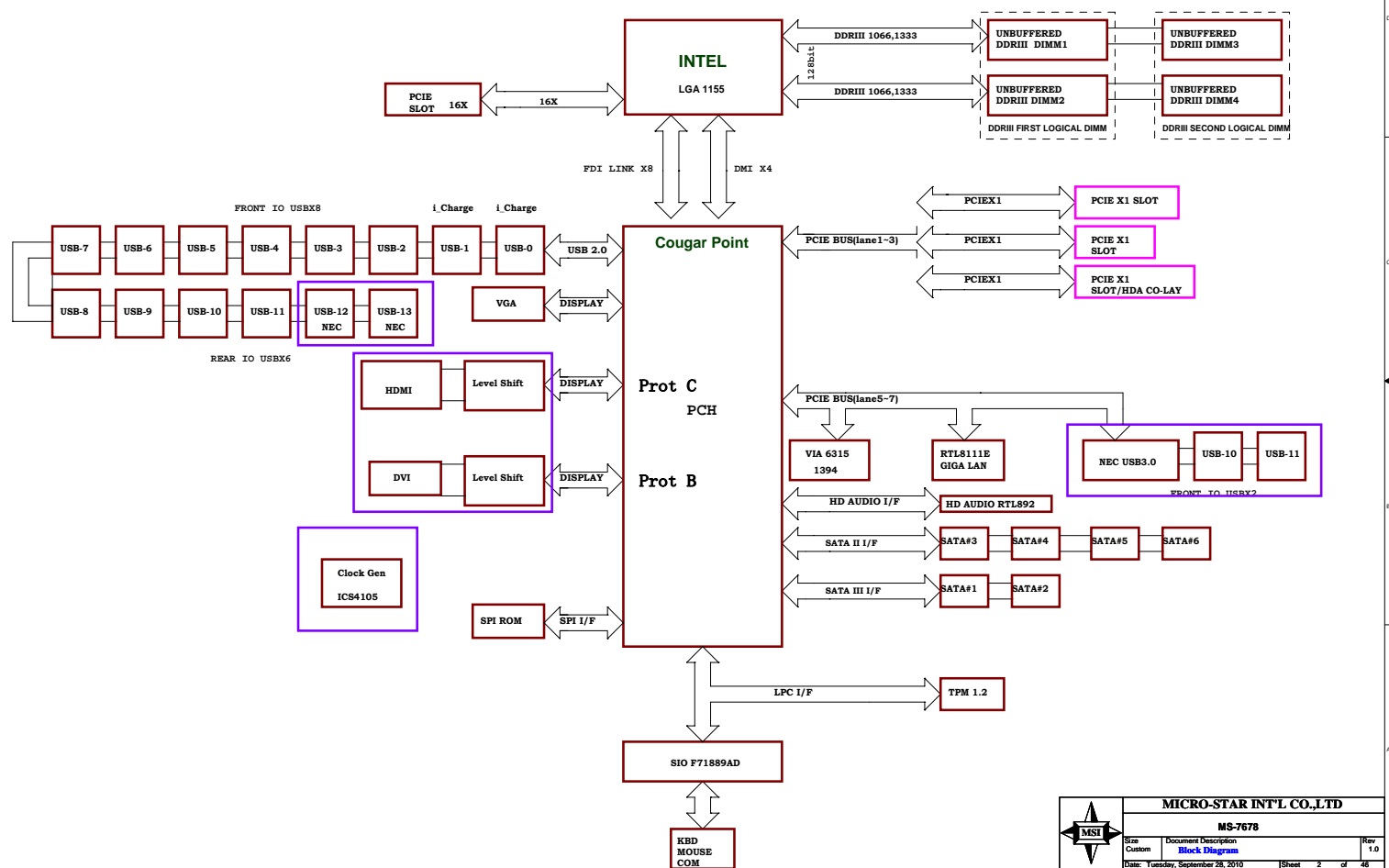
on BOARD BUZZER

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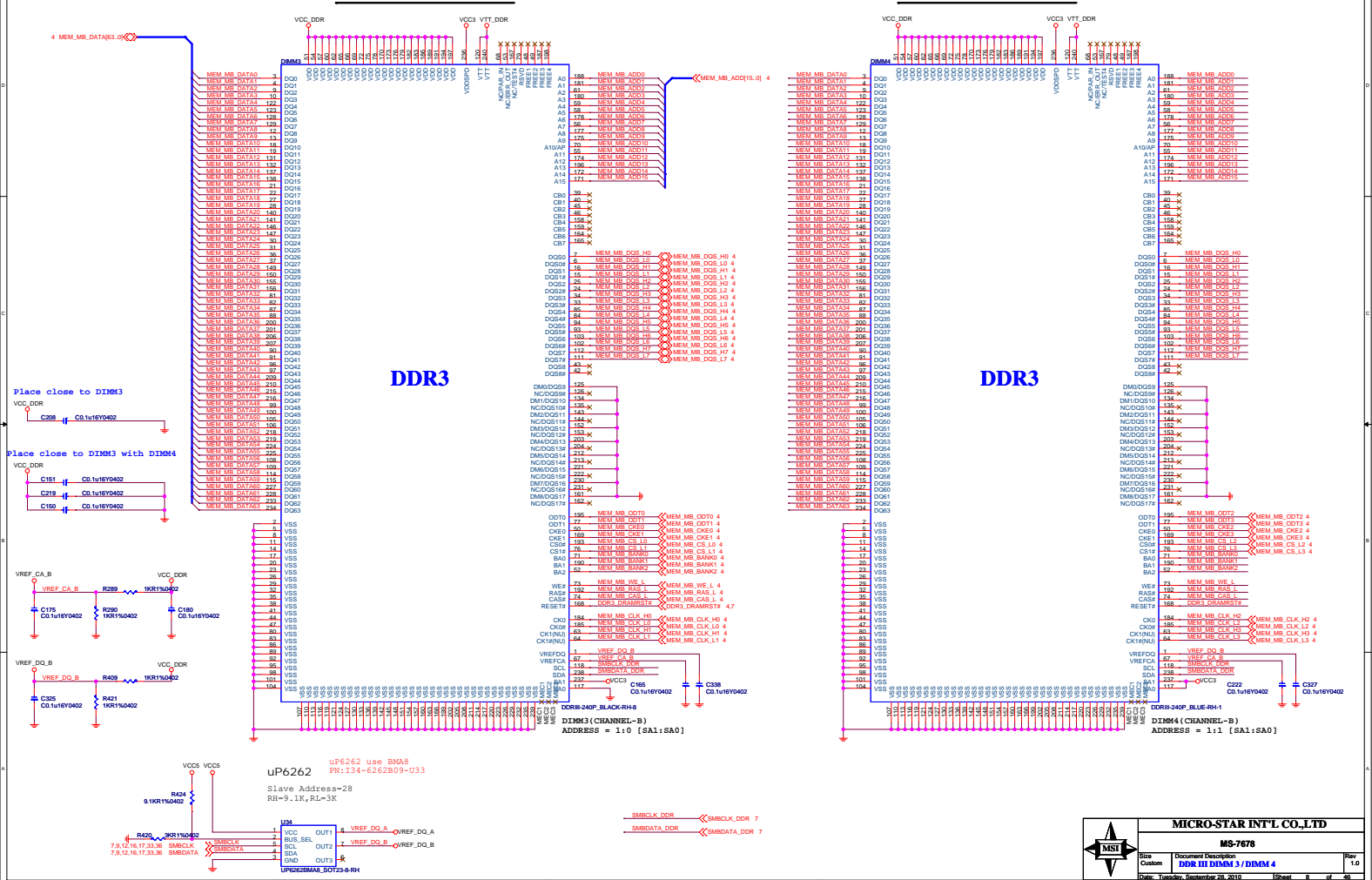


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DDRIII DIMM A1

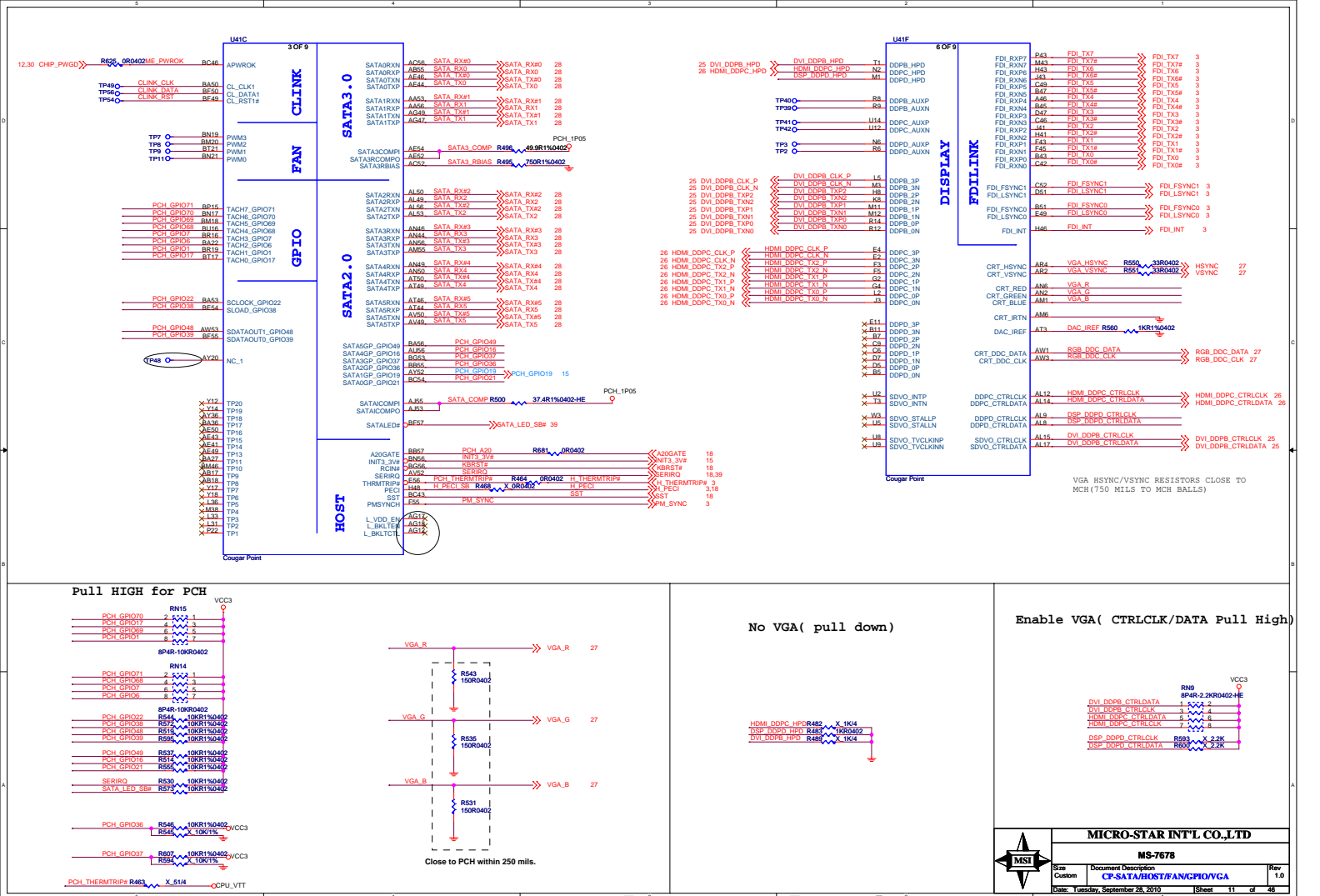
DDR3 DIMM B0

DDR3 DIMM B1

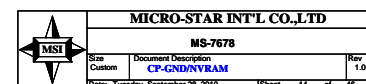


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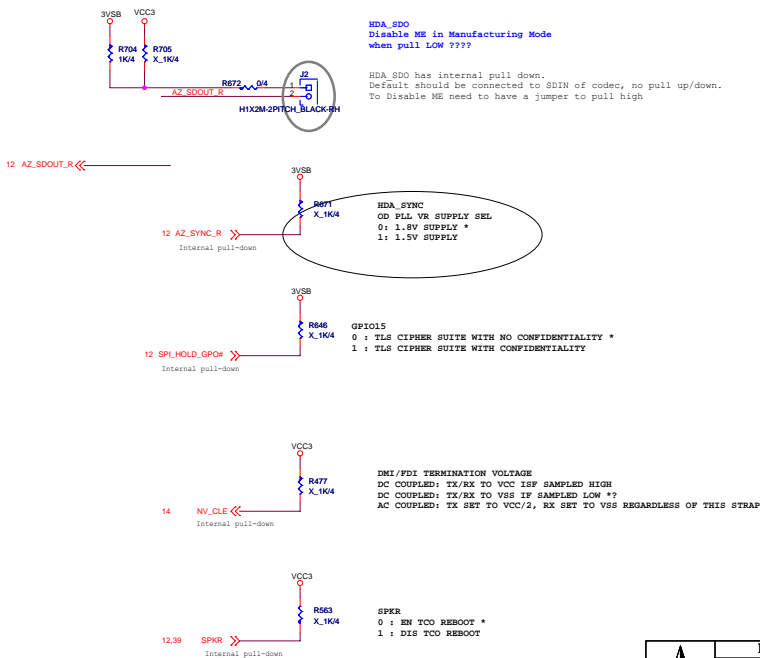
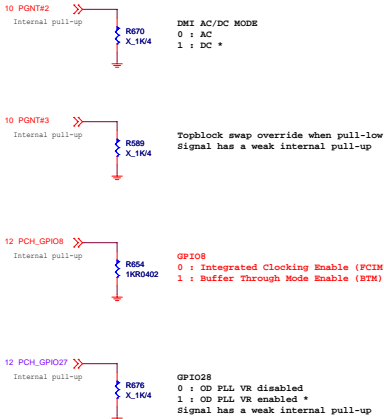
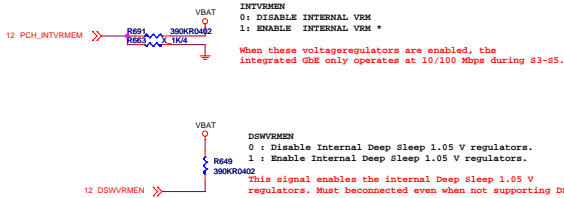
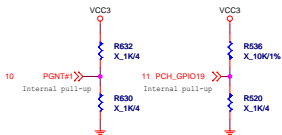


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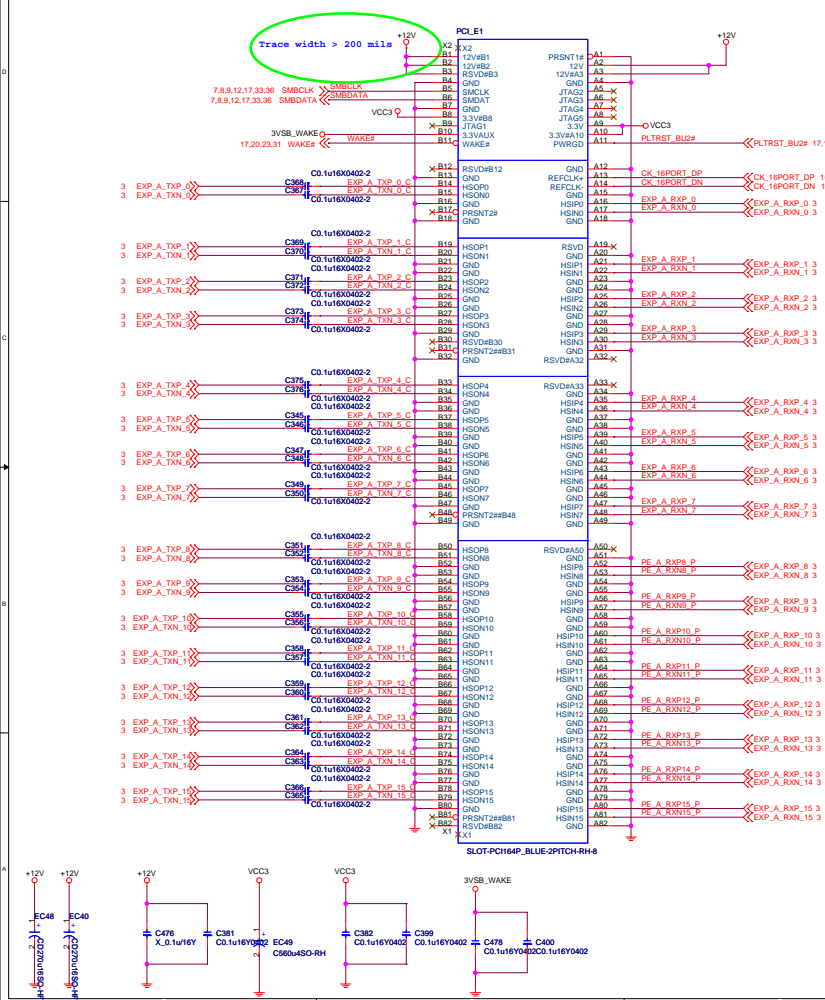
PCH Straps

BOOT DEVICE	GNT1	SATA/GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

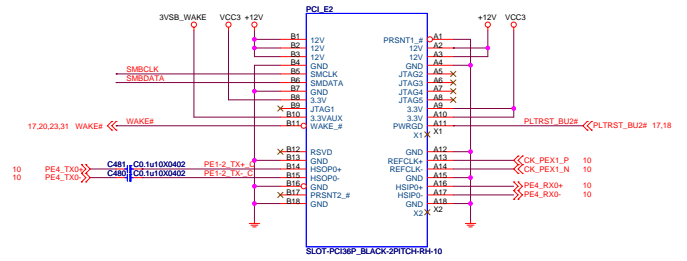


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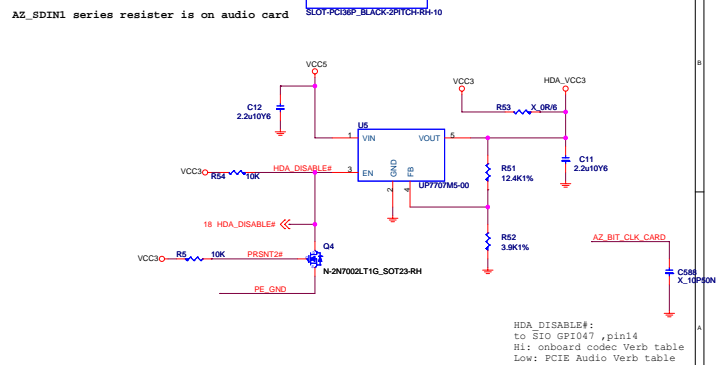
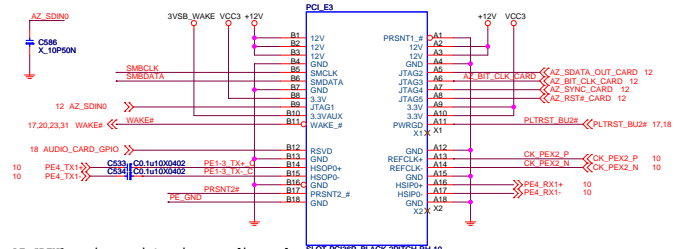
PCI_Express X16 slot



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

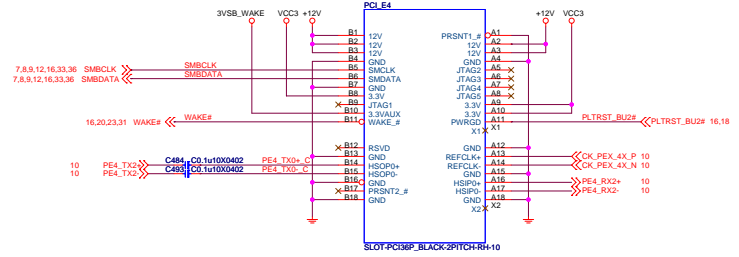


	PE1X1_PRSENT#	PE_GND
Other board	0	0
4132 audio	1	0
N/A	1	N/C

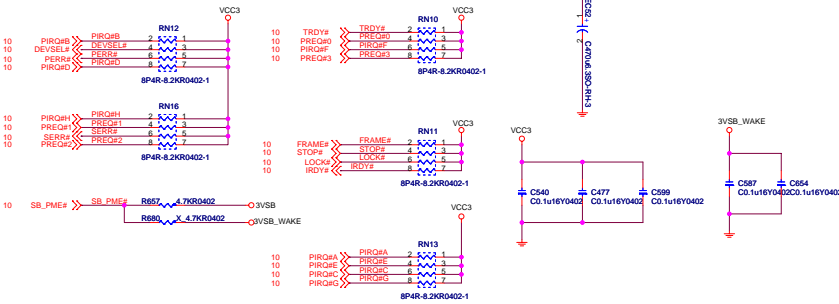


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PCI EXPRESS x1-PORT

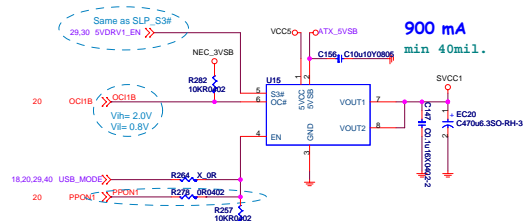
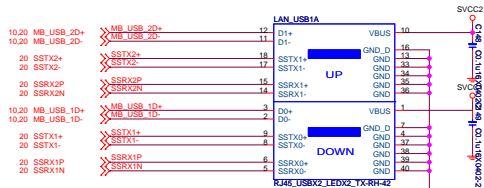


PCI PULL-UP / DOWN RESISTORS

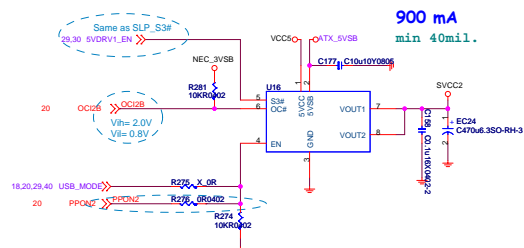


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All power sources of uPD720200 are supplied, PPOnx is enable.
PPOnx is low when OC1x going to low.

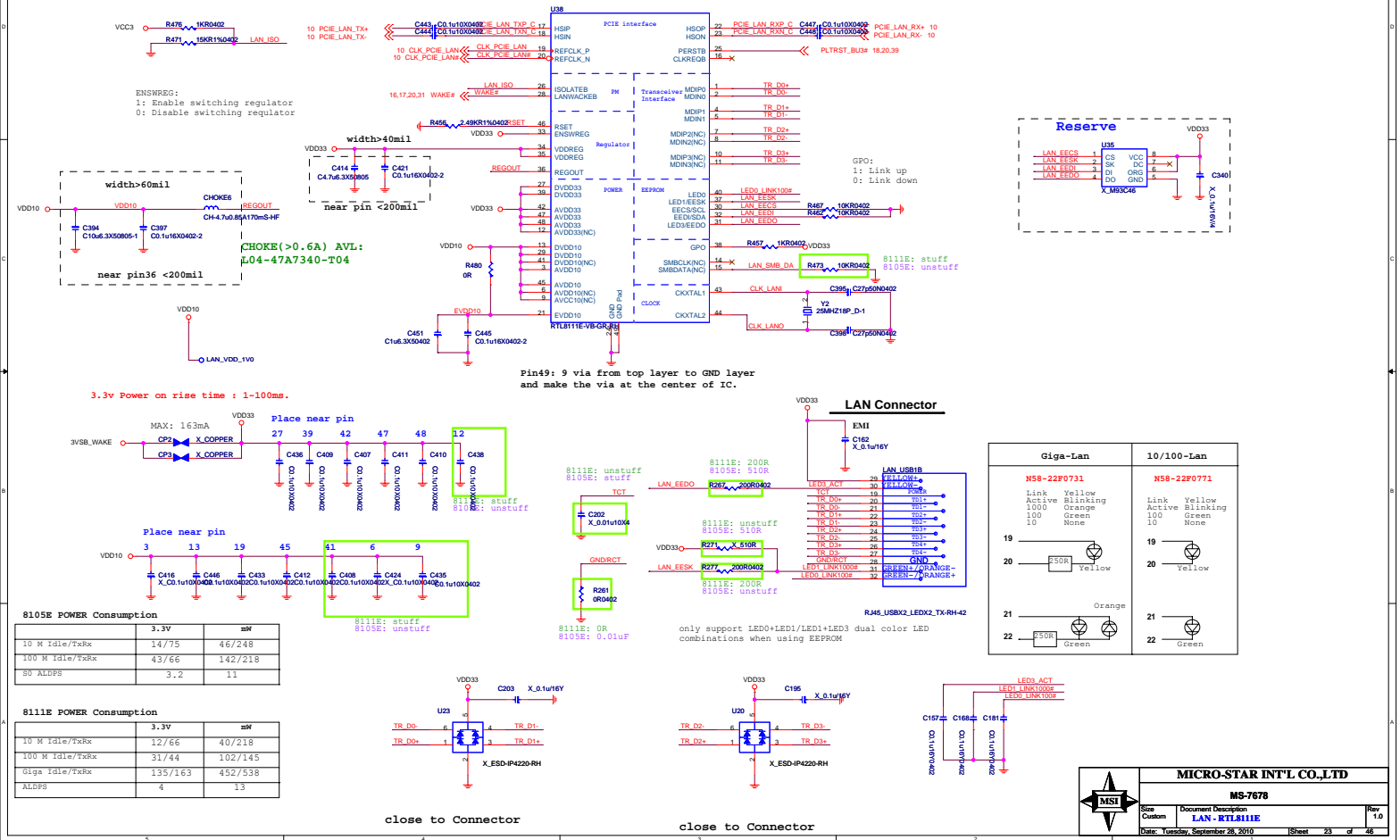


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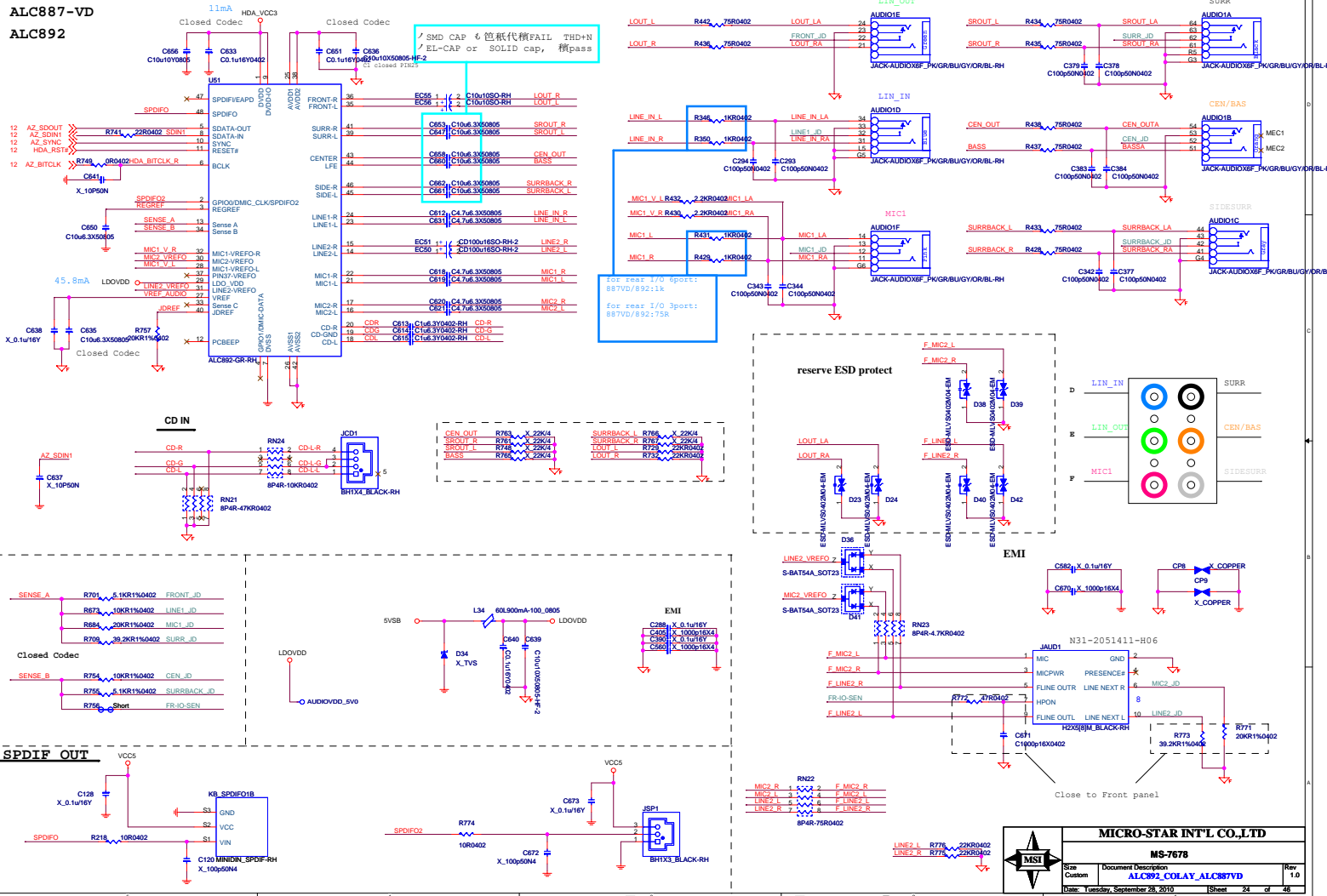
RTL8111E Giga LAN

RTL8105E 10/100M LAN



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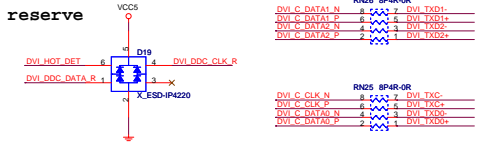
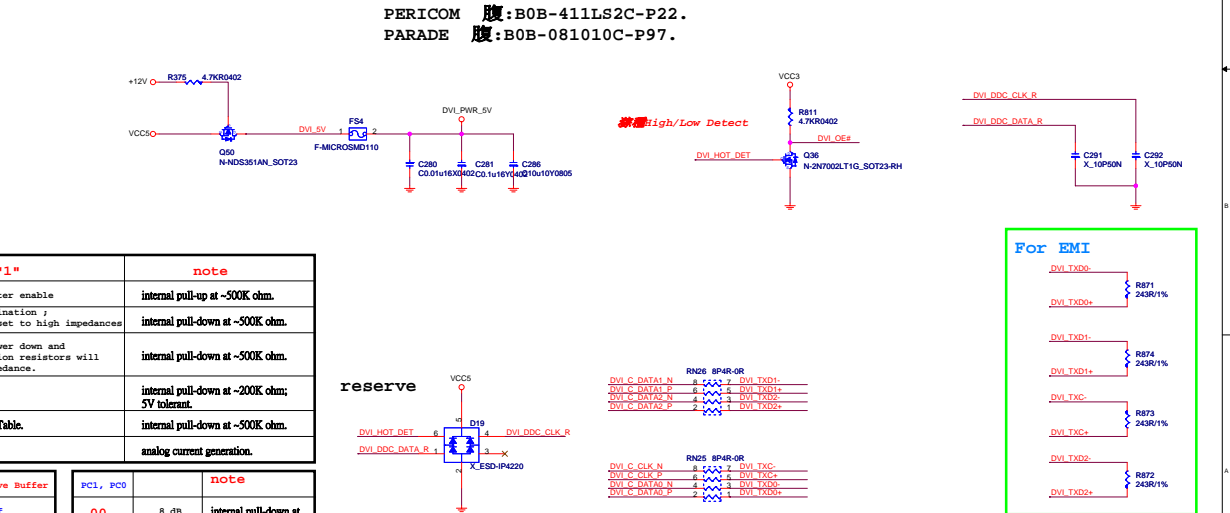
ALC887-VD ALC892




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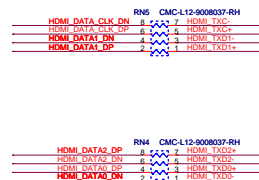
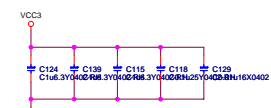
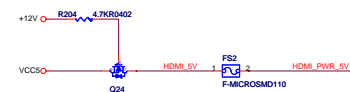
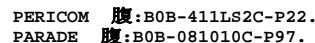
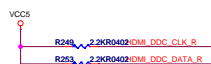
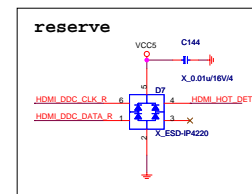
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCRUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
RESET			analog current generation.


DDC_EN, DDCRUF_EN, OE#	DDC Passive Switch	DDC Active Buffer	PC1, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB



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11	HDMI_DDPCK_CLK_P	HDMI_DDPCK_CLK_P
11	HDMI_DDPCK_CLK_N	HDMI_DDPCK_CLK_N
11	HDMI_DDPCK_TX2_P	HDMI_DDPCK_TX2_P
11	HDMI_DDPCK_TX2_N	HDMI_DDPCK_TX2_N
11	HDMI_DDPCK_TX1_P	HDMI_DDPCK_TX1_P
11	HDMI_DDPCK_TX1_N	HDMI_DDPCK_TX1_N
11	HDMI_DDPCK_TX0_P	HDMI_DDPCK_TX0_P
11	HDMI_DDPCK_TX0_N	HDMI_DDPCK_TX0_N

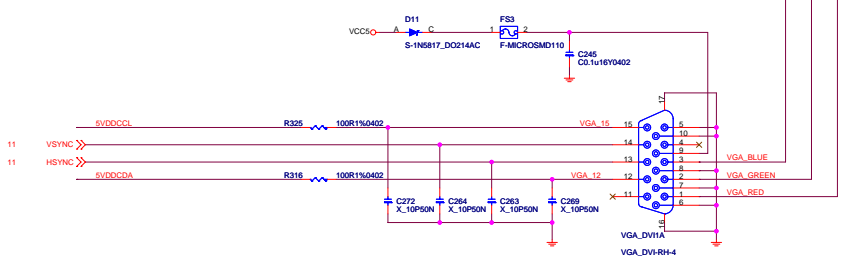
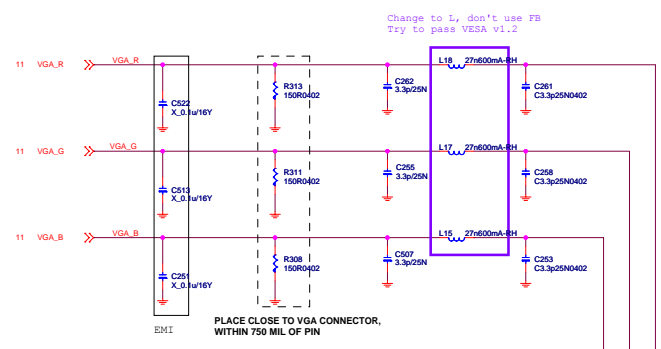
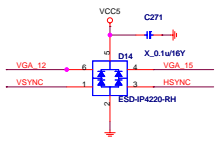
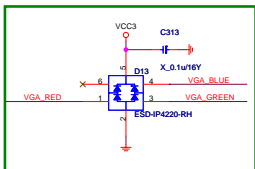
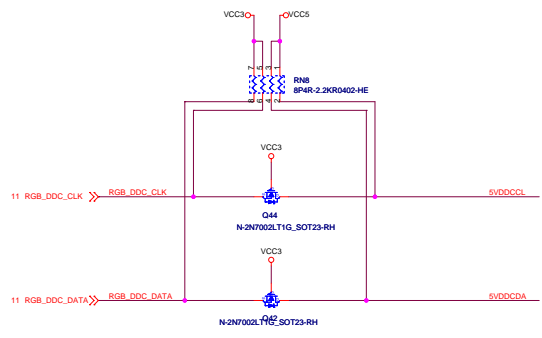


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D-Sub

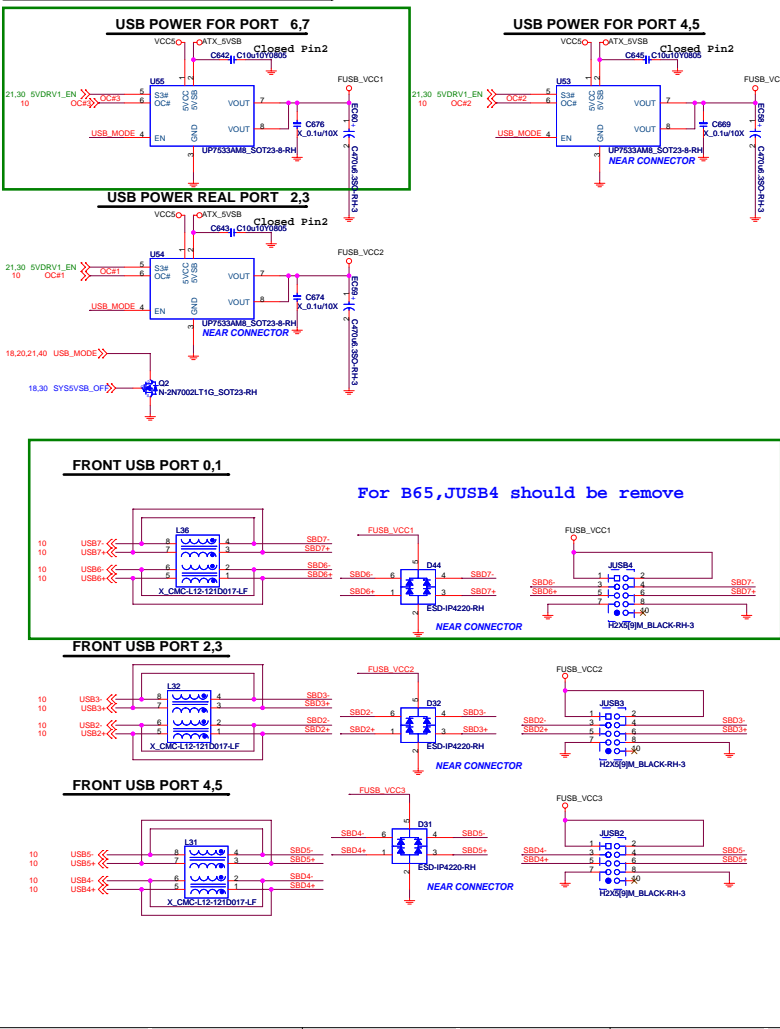
Level shift



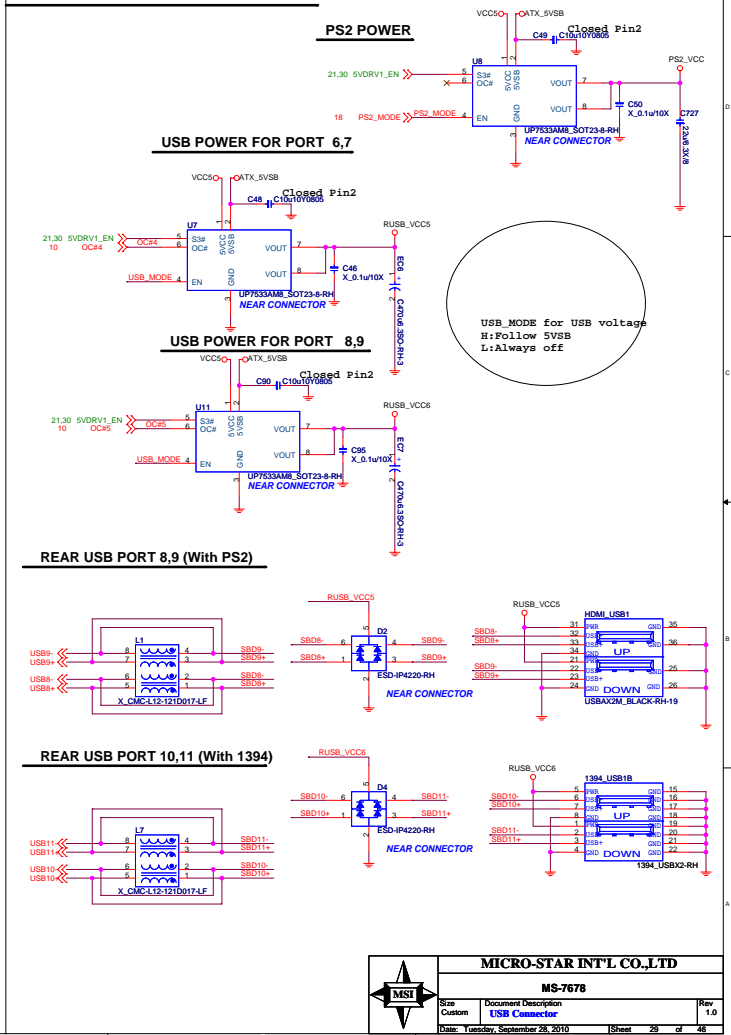
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Front USB Connector

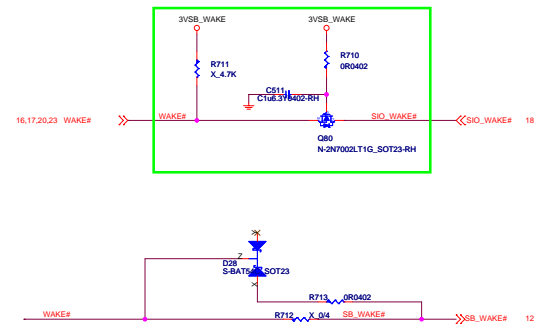


Rear USB Connector

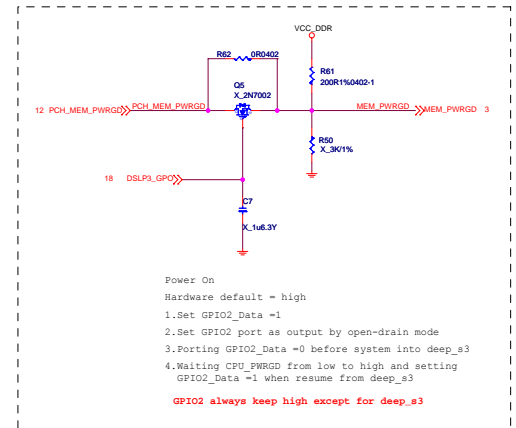



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LAN/PCIE/PCI Wake Up CTRL Circuit



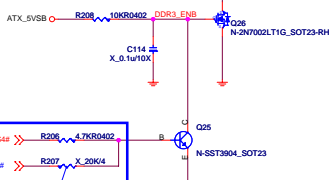
APS & LED



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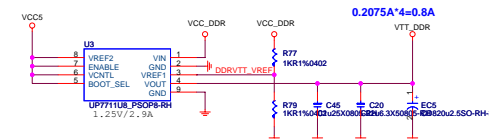
4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

Meet Intel power down sequence. DDR 0.9 REF R



For Deep S3 Mode

To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .

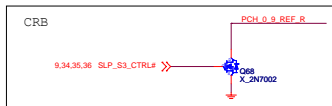



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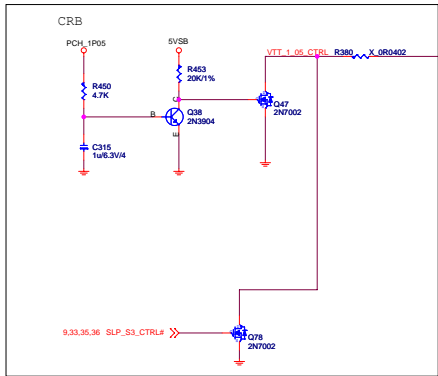
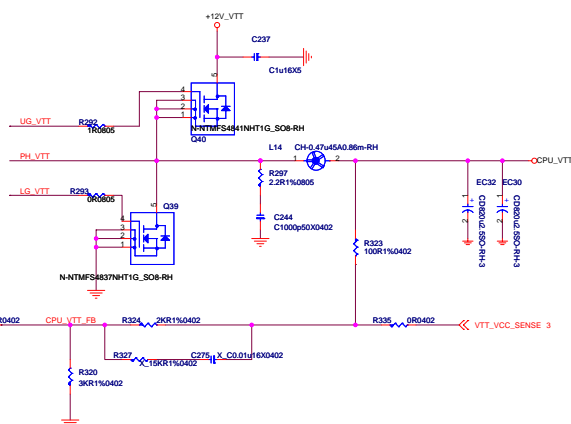
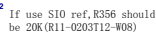
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SIO 0.9V REF

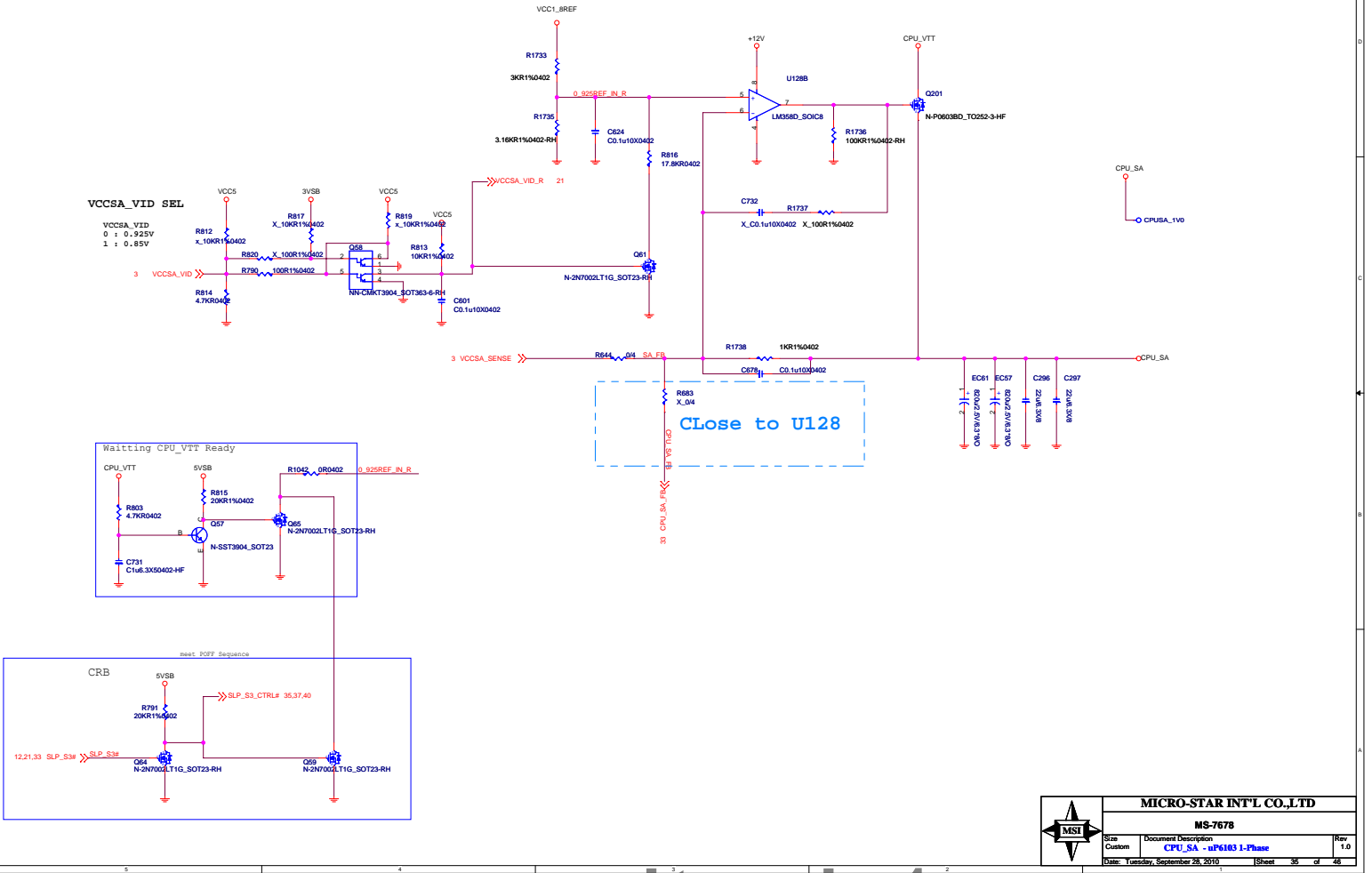


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CPU VTT 8.5A
8.5A FOR CPU

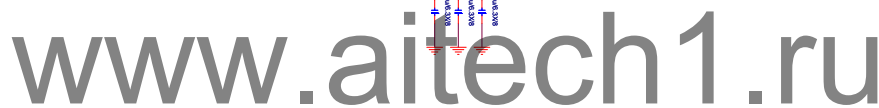
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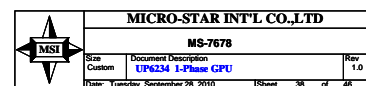
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Size Custom	Document Description CPU_VTT - uP6103- 1-Phase		Rev 1.0
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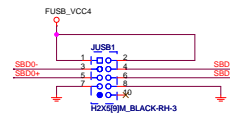
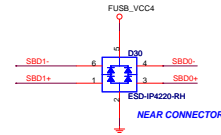
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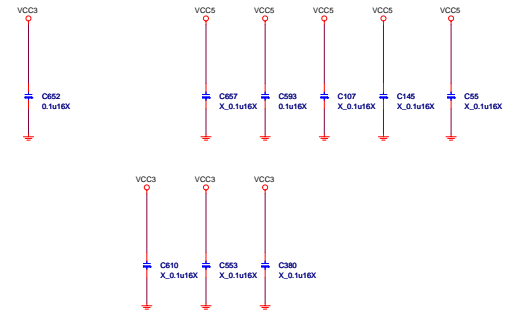


The schematic diagram illustrates the USB-to-serial converter circuit. On the left, four USB signal lines are shown: USB1- and USB1+ (top two), and USB0- and USB0+ (bottom two). These lines are connected to the pins of the XMC-L12-121D017-LF chip. Specifically, USB1- connects to pin 8, USB1+ to pin 7, USB0- to pin 4, and USB0+ to pin 3. The chip is also connected to a serial interface on the right, with S80D1- and S80D1+ connected to pins 2 and 1, and S80D0- and S80D0+ connected to pins 4 and 3. The chip is labeled 'L30' and 'XMC-L12-121D017-LF'.

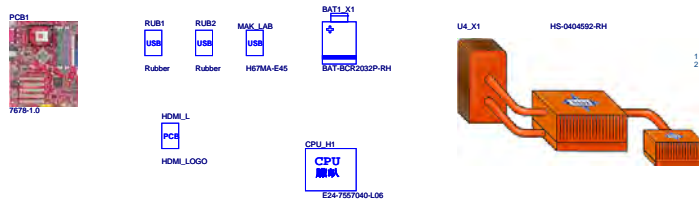


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PCH XDP



PCH XDP PWRGD/RESET

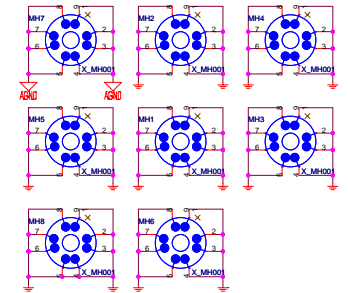
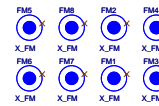


Mounting Holes

Simulation



Optical Fiducial Marks-120



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